REMARKS

In response to the Office Action dated June 4, 2002, claim 1 has been amended. Claims 1-8 are active in this application, of which claim 1 is independent. Claims 2-6 have been indicated as allowable but objected to for being dependent from a rejected base claim.

Entry of the Amendments and Remarks is respectfully requested because entry of Amendment places the present application in condition for allowance, or in the alternative, better form for appeal. No new matters are believed to be added by this Amendments. Based on the above Amendments and the following Remarks, Applicants respectfully request that the Examiner reconsider the outstanding objections and rejections and they be withdrawn.

Rejections Under 35 U.S.C. §103

In the Office Action, claims 1, 7 and 8 have been rejected under 35 U.S.C. §103(a) for being unpatentable over U. S. Patent No. 6,049,322 issued to Yoshikawa, *et al.* ("Yoshikawa") in view of U. S. Patent No. 5,973,660 issued to Hashimoto, *et al.* ("Hashimoto"), further in view of U. S. Patent No. 5,777,610 issued to Sugimoto, et al. ("Sugimoto"). This rejection is respectfully traversed.

In the previous Amendment, Applicants argued that "Yoshikawa teaches the first and second groups of wires are overlapping each other, but fails to teach or suggest the first and second groups of wires positioned separately from each other, as claimed" (Page 3, lines 3-5).

In response to this argument, the Examiner stated that "Claim 1 ... does not explicitly state where the wire must not overlap, only that they be "positioned separately". Examiner

contends that "positioned separately" could conceivably be determined to be where the wires are not from the same FIFO, thus Yoshikawa clearly discloses where the first group of wires and the second group wires are positioned separately" (Office Action, Page 4, Line 19 to Page 5, Line 2).

In this response, claim 1 has been amended to recite "the first group of wires are *entirely spaced apart* from the second group of wires" to clarify the difference between the claimed invention and the applied references.

As previously mentioned, due to the intended wiring arrangement, in Yoshikawa, the group of wires extended from the FIFO-E 7 (i.e., first group of wires) *must overlap* the group of wires extended from the FIFO-O 9 (i.e., second group of wires) at certain locations. Thus, in Yoshikawa, it would *never* be possible for the groups of wires to be *entirely spaced apart* from each other. For example, Fig. 1 of Yoshikawa shows the group of wires from the FIFO-E 7 connected to the source driver 15 *overlapping* the group of wires from the FIFO-O 9 connected to the source drivers 13 and 17. Thus, it is respectfully submitted that Yoshikawa fails to teach or suggest that "the first group of wires are *entirely spaced apart* from the second group of wires".

As previously mentioned, the secondary references to Hashimoto and Sugimoto fails to cure the deficiency from the teachings of Yoshikawa. Thus, it would not have been obvious to combine the teachings of the applied prior art references to arrive at the claimed invention.

In fact, Yoshikawa is directed to a method called "frequency division", in which a first image signal bus is coupled to all the odd numbered source drive ICs and a second image signal bus is coupled to all the even numbered source driver IC. As described in the Description of the Related Art, in the frequency division method, "the buses for transmitting such image signal should be arranged along the same direction from the first source drive IC to the tenth source

drive IC, which causes the *coupling effect* with the adjacent image signals by a parasitic capacitance, thereby *delaying the signal transmission*" (Specification, Page 2, Lines 19-22). The present invention is directed to solving this problem by forming the first group of wires and the second group of wires on different regions of the source PCB 20 such that "the first group of wires are *entirely spaced apart* from the second group of wires", as recited in claim 1. Thus, it should be noted that the claimed invention provides the solution to the problems of Yoshikawa.

For the reasons above, Applicants respectfully submit that claim 1 is patentable over Yoshikawa, Hashimoto and Sugimoto. Likewise, claims 7 and 8, that are dependent from claim 1, would be also patentable at least for the same reason. Accordingly, Applicants respectfully request that all the rejections and objections over claims 1, 7 and 8 be withdrawn.

CONCLUSION

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, claims 1-8 are in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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APPENDIX

The "marked-up" version of the amended claim is as follows:

1. (Amended) A liquid crystal display, comprising:

a signal processor for generating and outputting a first image signal and a second image signal, a gray scale voltage, a gate voltage, and a driving control signal using an image data, a main control signal, and a power source all of which are supplied from an image supplying source, the driving control signal including a source driving control signal and a gate driving control signal;

a data signal driver for generating and outputting a data signal from the first image signal and the second image signal, the gray scale voltage and the source driving control signal all of which are input from said signal processor;

a printed circuit board having a plurality of wires for transmitting the signals and/or voltages of said signal processor to said data signal driver;

a gate signal driver for generating and outputting a gate signal from the gate voltage and the gate driving control signal of said signal processor; and

a liquid crystal display panel for displaying an image formed by receiving the data signal from said data signal driver and the gate signal from said gate signal driver,

wherein the plurality of wires comprises a first group of wires for transmitting the first image signal and a second group of wires for transmitting the second image signal, and the first group of wires are [positioned separately] <u>entirely spaced apart</u> from the second group of wires.